CLAIMS

We claim:

1. An integrated circuit including a first inductance structure on a semiconductor substrate, intended for operating at frequencies greater than several hundreds of MHz, comprising:

a first inductance formed by a conductive track having first and second ends and having first and second terminals connected, respectively, to the first and second ends of the conductive track;

a second inductance formed by the conductive track between the second terminal and an intermediate point of the conductive track connected to a third terminal, said second and third terminals forming two terminals of the second inductance; and

means for setting the third terminal to high impedance when the first inductance is used.

2. The circuit of claim 1, wherein the conductive track is formed of rectilinear segments.

3. The circuit of claim 2, wherein the conductive track is substantially of octagonal shape.

4. The circuit of claim 1, wherein said intermediate point is connected to the third terminal via a rectilinear conductive segment.

5. The circuit of claim 4, wherein said conductive segment is substantially perpendicular to the conductive track.

6. The circuit of claim 1, including a second inductance structure symmetrical to the first inductance structure and including:

a first inductance formed by a conductive track having first and second ends and having first and second terminals connected, respectively, to the first and second ends of the conductive track;

a second inductance formed by a portion of the conductive track between the second terminal and an intermediate point of the conductive track connected to a third terminal, said second and third terminals forming two terminals of the second inductance; andmeans for setting the third terminal to high impedance when the first inductance is used;

wherein the conductive tracks of the first and second structures are interleaved so that the two conductive tracks have the same length, and wherein the distances from each of the intermediary points of each of the conductive tracks of the first and second structures of inductances to the respective second ends of said conductive tracks are equal.

7. The circuit of claim 6, wherein the conductive tracks of the first and second structures of inductances share a common second end and second terminal.

8. The circuit of 6, further including first and second processing chains, the first chain including a first mixer adapted to using a first frequency and the second chain including a second mixer adapted to using a second frequency, the first terminal of the first structure of inductances being connected to the first mixer, the second terminal of the first structure of inductances being connected to a circuit ground, and the third terminal of the first structure of inductances being connected to the second mixer.

9. The circuit of claim 6, wherein the first terminal of the second structure of inductances being connected to the first mixer, the second terminal of the second structure of inductances being connected to the circuit ground, and the third terminal of the second structure of inductances being connected to the second mixer.

10. A method, comprising:

receiving a first signal modulated on a first carrier frequency;

demodulating the first signal using a circuit that includes first and second inductors formed on a semiconductor substrate, the first and second inductors including first and second conductive tracks, each track having first and second terminals connected to the respective conductive tracks at first and second ends thereof;

receiving a second signal modulated on a second carrier frequency; and

demodulating the second signal using a circuit that includes third and fourth inductors formed on a semiconductor substrate, where the third inductor is a portion of the first inductor, defined by a segment of the first conductive track between the second terminal of the first conductive track and a third terminal of the first conductive track, connected to an intermediate point of the first conductive track, and the fourth inductor is a portion of the second inductor, defined by a segment of the second conductive track between the second terminal of the second conductive track and a third terminal of the second conductive track, connected to an intermediate point of the second conductive track.

11. The method of claim 10 wherein, while the demodulating the first signal step is performed, the third terminals of the first and second conductive tracks are maintained at high impedance.

12. The method of claim 10 wherein the first and second inductors are of equal inductive value, and the third and fourth inductors are of equal inductive value.

13. The method of claim 10, wherein the first and second conductive tracks are interleaved so that the two conductive tracks have the same length, and wherein the distances from each of the third terminals of the first and second conductive tracks to the respective second terminals of the conductive tracks are equal.

14. The method of claim 13 wherein the first and second conductive tracks share a common second end and second terminal.